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Attachment (English translation of the Citation)

Publication No.: 295728
Publication Date: July 11, 1997
Application No.: 84113408
Filing Date: December 15, 1995
Patent No.: NI-083240
Title: Thin-film transistor and its manufacturing method
Inventors: A Japanese and an American
Applicants: Sharp Co. Ltd. (Japan) and Three angles Research Institute (America)

Claims:

1. A thin-film transistor, it has an insulation-body, which is held between a gate and a polysilicon semiconductor, said polysilicon semiconductor includes a source-region, a drain-region and a channel between said two regions, characterized in that:
   a boundary oxide-layer, which is contacted with said polysilicon semiconductor layer,
   a cap oxide-layer, which is contacted with said gate,
   a nitride-layer, which is held between said boundary oxide-layer and said cap oxide-layer.
2. A thin-film transistor according to claim 1, wherein said boundary oxide-layer is an SiO2-lalyer, said cap oxide-layer is an SiO2-lalyer, and said nitride-layer is an Si3N4-lalyer.
3. A thin-film transistor according to claim 1, wherein the thickness-ratio of the boundary oxide-layer to the nitride-layer is large enough to prevent the electronic traps from forming on the boundary between said polysilicon and said boundary oxide-layer.
4. A thin-film transistor according to claim 1, wherein the thickness-ratio of the boundary oxide-layer to the nitride-layer is 2:1.
5. A thin-film transistor according to claim 1, wherein the thickness-ratio of the boundary oxide-layer, the nitride-layer and the cap oxide-layer is 10:5:85.
6. A manufacturing method for a thin-film transistor, it includes the following steps: source-regions and drain-regions are formed on polysilicon semiconductor-layer coated on a substrate,ONO-insulation structures are formed on said polysilicon semiconductor-layer, and gates are formed on said ONO-insulation structures.
7. A method according to claim6, wherein the steps for producing said ONO-insulation layers are:
   a boundary oxide-layer is formed on said polysilicon semiconductor-layer,
   a nitride-layer is formed on said boundary oxide-layer,
   a cap oxide-layer is formed on said nitride-layer.
8. A method according to claim 7, wherein said boundary oxide-layer is an SiO2-lalyer, said cap oxide-layer is an SiO2-lalyer, and said nitride-layer is an Si3N4-lalyer.

9. A method according to claim 7, wherein the thickness-ratio of the boundary oxide-layer to the nitride-layer is large enough to prevent the electronic traps from forming on the boundary between said polysilicon and said boundary oxide-layer.
10. A method according to claim 7, wherein the thickness-ratio of the boundary oxide-layer to the nitride-layer is 2:1.
11. A method according to claim 7, wherein the thickness-ratio of the boundary oxide-layer, the nitride-layer and the cap oxide-layer is 10:5:85.

Fig. 1 Section view of a TFT with ONO-insulation according to the 1st embodiment of this invention.
Fig. 2 Section view of a TFT with ONO-insulation according to the 1st (inverted) embodiment of this invention.
Fig. 3 Section view of a semiconductor memory device.
Fig. 4 Section view of a previous TFT.

Figure 1

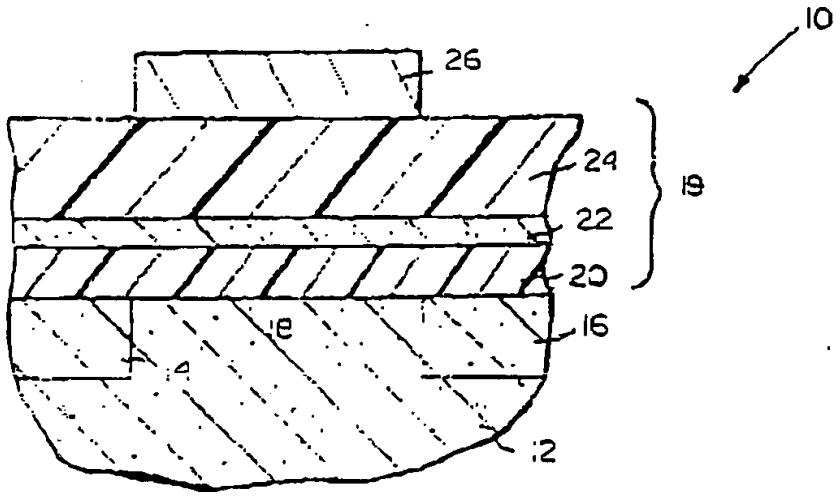


Figure 2

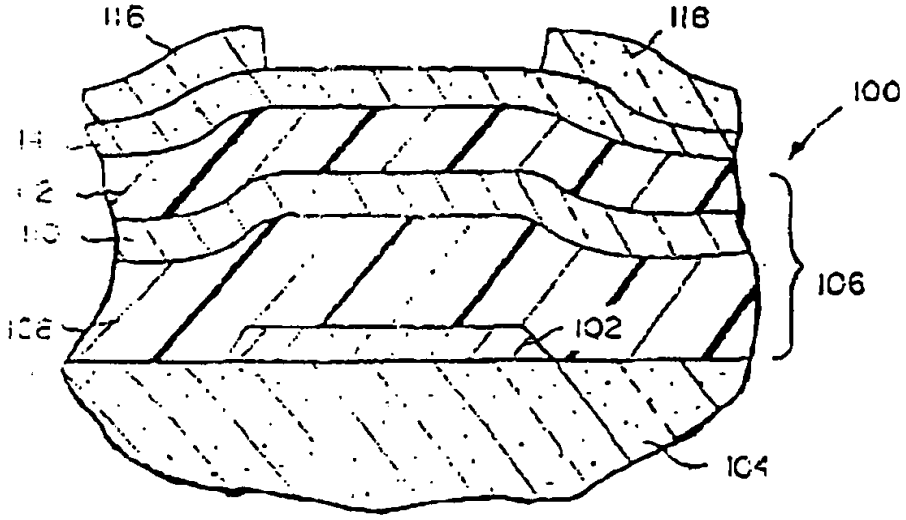


圖 3 Figure 3.

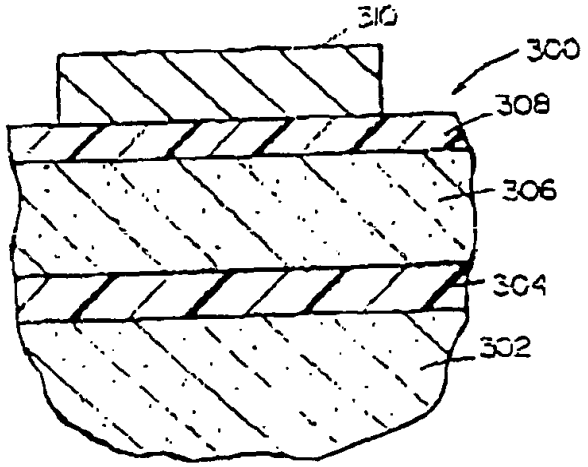
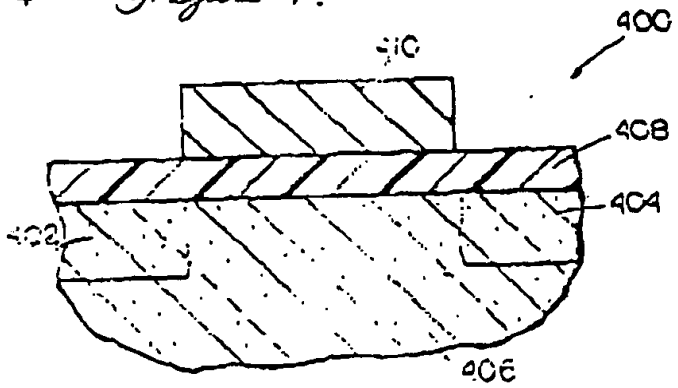


圖 4 Figure 4.



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English Translation of

DECISION ON EXAMINATION

Date: June 24, 2002
No.: 04039/09183010423

1. Application No. 90119349
2. Title: Speicherzelle, Speicherzellenanordnung und Herstellungsverfahren
3. Applicant: Infineon Technologies AG
4. Attorneys: Ted C.T. Ho and Ming-Yi Lee
   Address: 8F, Chung Ting Building, No. 77, Tun Hwa S. Rd., Sec. 2, Taipei, Taiwan, R.O.C.
5. Filing Date: August 8, 2001
6. Priorities: 1. 2000/08/11 DE100 39 441.8
   2. 2001/07/06 US09/900,654
7. Decision:

A) Subject:

A patent should not be granted to this application.

B) Basis:

Paragraph 2 of Article 20 of the Patent Law.

C) Reasons:

After examination, the present case is deemed that:

1. The main feature of the present case has been described in claim 1.
2. Some features similar to the present case are found in Publication No. 295728 published on January 11, 1997 which entitled "Thin-film transistor and its manufacturing method" (please see the attachment), in which according to claim 6 a source-region and a drain-region are mounted on a polysilicon semiconductor-layer coated on a substrate; after an ONO-insulation Structure is formed on said polysilicon semiconductor-layer, a gate-electrode is formed. In the present case, the ONO-layer existed either between a source-region and a gate-electrode or between a drain-region and a gate-electrode only belongs to the already known technique or knowledge in the cited case.

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Such a technique can easily be accomplished by any one skilled in that art, so the present case has no inventive steps.

Summing up the above, the present application does not comply with the legal requirements of a patent. The Decision is hereby made as per Subject according to Paragraph 2 of Article 20 of the Patent Law.

Note: If the applicant disagrees with this decision, a re-examination can be filed within thirty days after receipt of this decision with respondent reasons in duplicate and official fee of NT$6,000 (for Chinese specification and drawings under 50 pages, in case of exceeding 50 pages, additional fee of NT$500 per 50 pages shall be surcharged) to this Office.

OUR COMMENTS:

An ONO-insulation structure is described in the cited Publication No. 295728 (please see the attachment, it includes 11 claims and 4 figures). Though an ONO-layer sequence is also disclosed in the present case, the structure of the present case is clearly different from the cited case. We thus propose that a complete structure be described in claim 1. For example, numerals 1 to 7 have been disclosed in claim 1, we deem that other numerals such as 8 to 19 may also be disclosed in claim 1. In addition, it is better not to use indefinite words such as "zumindest (at least)".
We have duly translated the claims and figures of the said Citation into English, which are attached hereto for your review, reference and comparison.